计组2014考题

选择题：

1. the ------technology marked the start of the third generation computers。

Integrated-circuit 集成电路

1. which of the following additions will result in overflow in signed 2’s complement bimary interpretation 翻译of the result?
2. In the hardware circuit of implementing实施 Booth algorithm,the multiplier is placed 2m the Q register. And a 1-bit register Q-1 is placed cogically to the right of the least Rgnificant hit (Q0) of the Q register. The result of the multiplication whll appean 2n.The A and Q register .At the end of each cycle of computing the product,A,Q,Q-1 are ----- one bit position
3. Using 32-bit IEEE 754 shylc precision flooting point format to represent 0.6875.The exponent of the scale (E’)is-----
4. A word in a cache is retriered----
5. What characteristic of RAM memory makes it not suitable for permanent stange?
6. In a paging system,which of the following is not true?

11.In hardwared control unit,the uequrrel control signals are determined by the following information except----

15.once the PMA controller obtains access to the system bus, it tremsfors one byte of data and then returns the control of system bus to the processor. This is------

简答题

1. what is interrupt?what advantage does Interrupt-prirven I/O has over Program-controled I/O?
2. why do most of the computer systems today use”memory hierarchy”?
3. what are the advantage(s) and disadvantages of hardwired control unit?
4. Suppose a 32-bit instruction takes the following format

|  |  |  |  |
| --- | --- | --- | --- |
| opcode | Dest.reg | Src.reg | inmediate |

Assuming that there are 48 possible opcodes and 32 registers,what’s the range of numbers that can be represented by a two’s complent number in the immediate field?

应用题

1. conside the following 12-bit floating-point number representation format that is manageable for wenlaing through numerical.The first bit is the sign of the number,the next five bits represent on excess-15 exponent for the scale factor,which was an implied base of 2.The last six bits represent the fractional part of the mantissa,which has over implied 1 to the left of the bimary point.perform subtract operation on the operands.

A=0 10001 011011

B=1 01111 101010

Which represent the number A= +1,011011\*2^2 and B=-1,101010\*2^0.Note: using rounding as the truncation method in the answer the computation process?

1. consider a memory can be accessed with 20-bit address.Its word length is 64 bit and it is word-addressable.Assume that we use 256K\*8bit SRAM chip to constitute this memeory
2. how many byte can this memory store?
3. How many SRAM chips do we need?
4. How many address pims do need for chip select?why?
5. Draw a figure to cloow how this memory can be plenented using 256K\*8bit SRAM chip.
6. Give the sequence of cections needed to fetch and execute the instruction.

Load R5,x(R7)

Assume that the instruction is exeacted in a 127sc processor,and the clatapath figure is as follows:

RA,RB,RZ,RM

1. consider the following instructions at the given address in the memory:

1000 Add R3,R2,#20

1004 Subtract R5,R4,#3

1008 And Rb,R3,#0x3A

1012 Add R7,R2,R4

(1)Assume that the pipeline provides forwarding paths to the ALU from registors the flow of the mistuctions through the pipeline

(2)pescrible the contents of registors IR,PC,RA,RB,and RZ in the pipeline during cycles 2 to 8

5.A computer system has a cache organized in set associate manner.with 4 blocks per set and 64 words per block.The cache consist of 32 blocks and the main memory consist of 1024 blocks.The main memory is word-addressable.

1. how many bits are there in main memory
2. calculate the number of bits in each of the TAG.SET and WORD field of the main memory address format.
3. Assumeing that the cache is initially empty.The processor fetches 3072 words sequentially from main memory locations 0,1,….,3071,assume that the LRU algorithm is used for block replacement ,coupute the hit rate of this cache.